

Fig. 1 (Prior Art)



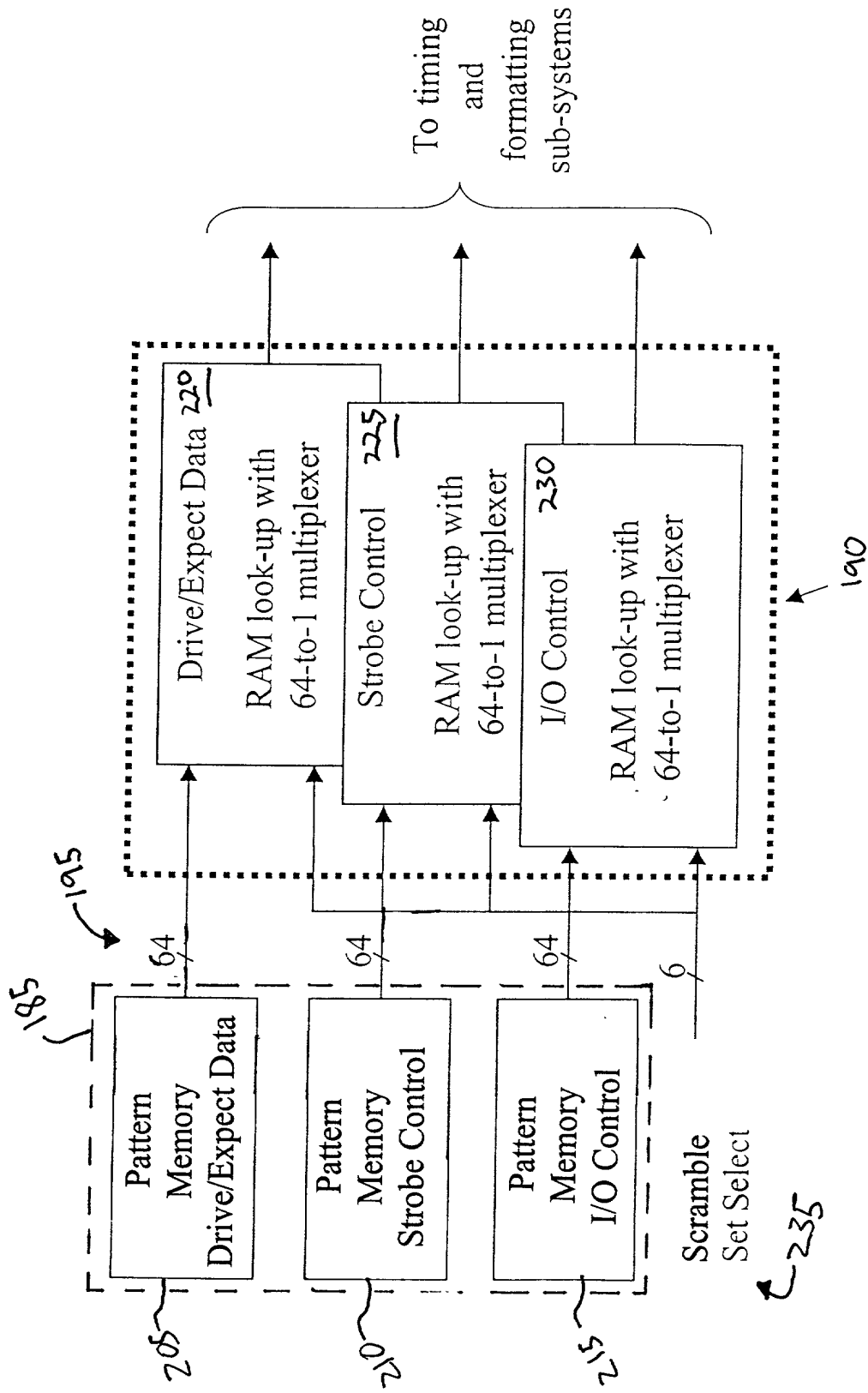


FIG. 3

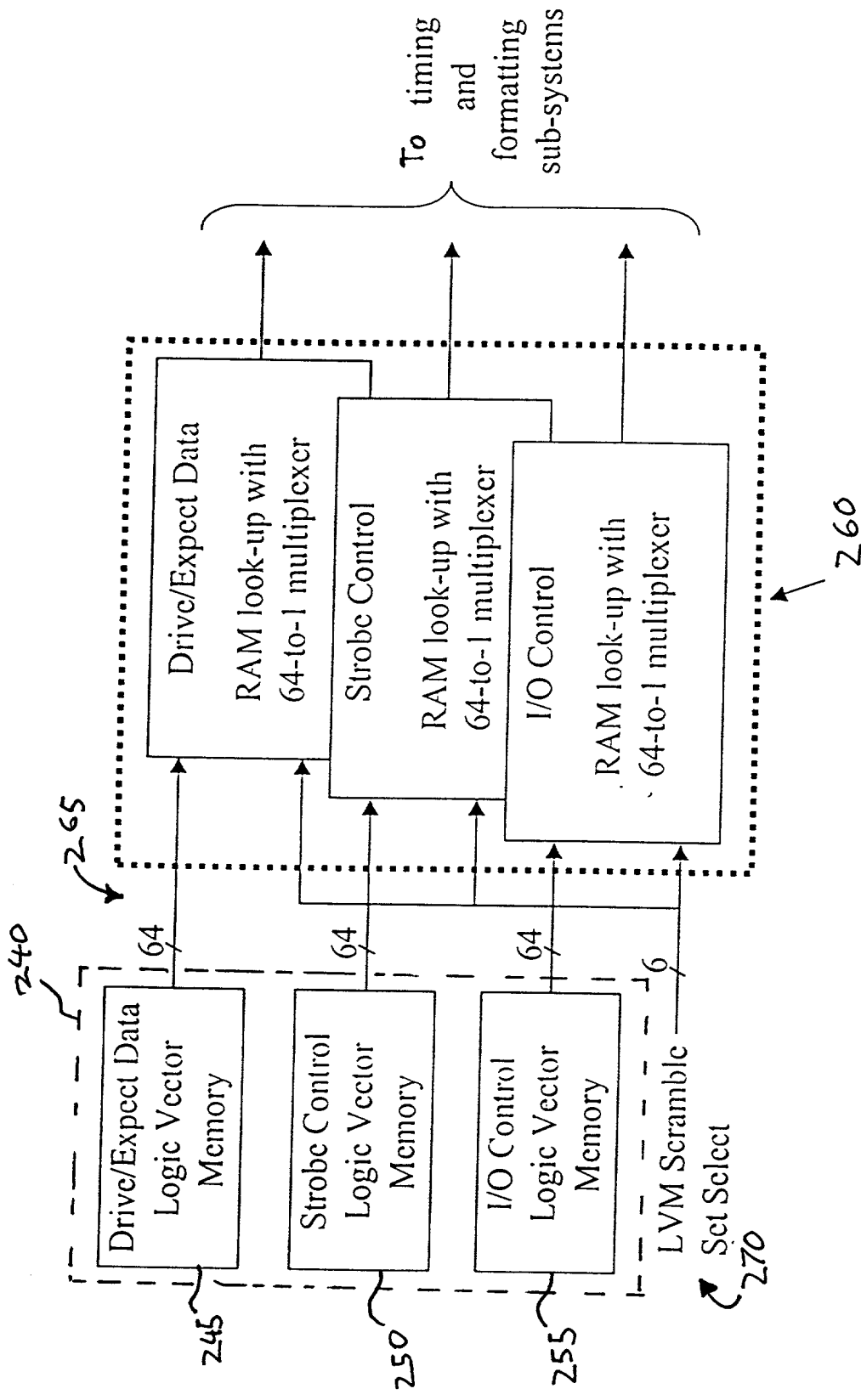


FIG. 4

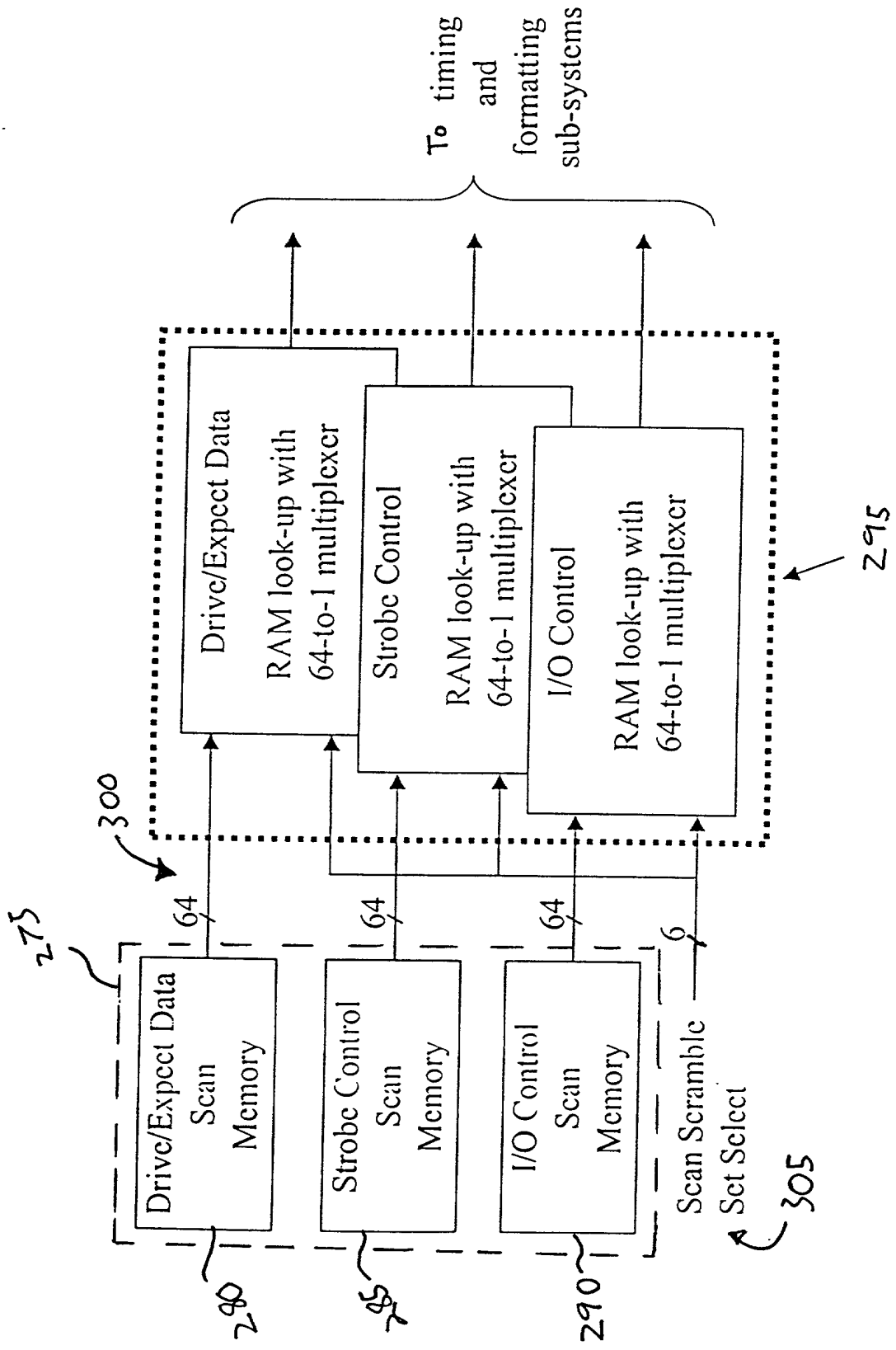


FIG. 5

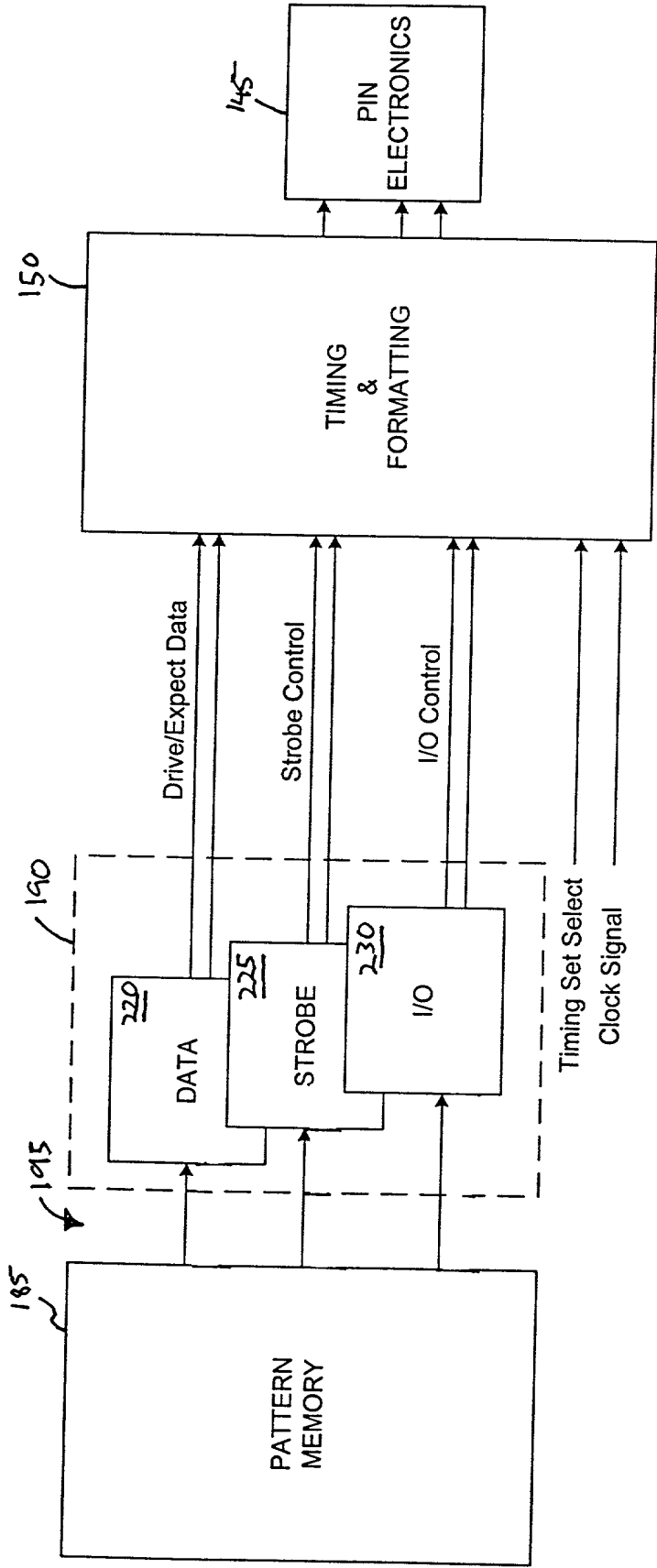


Fig. 6

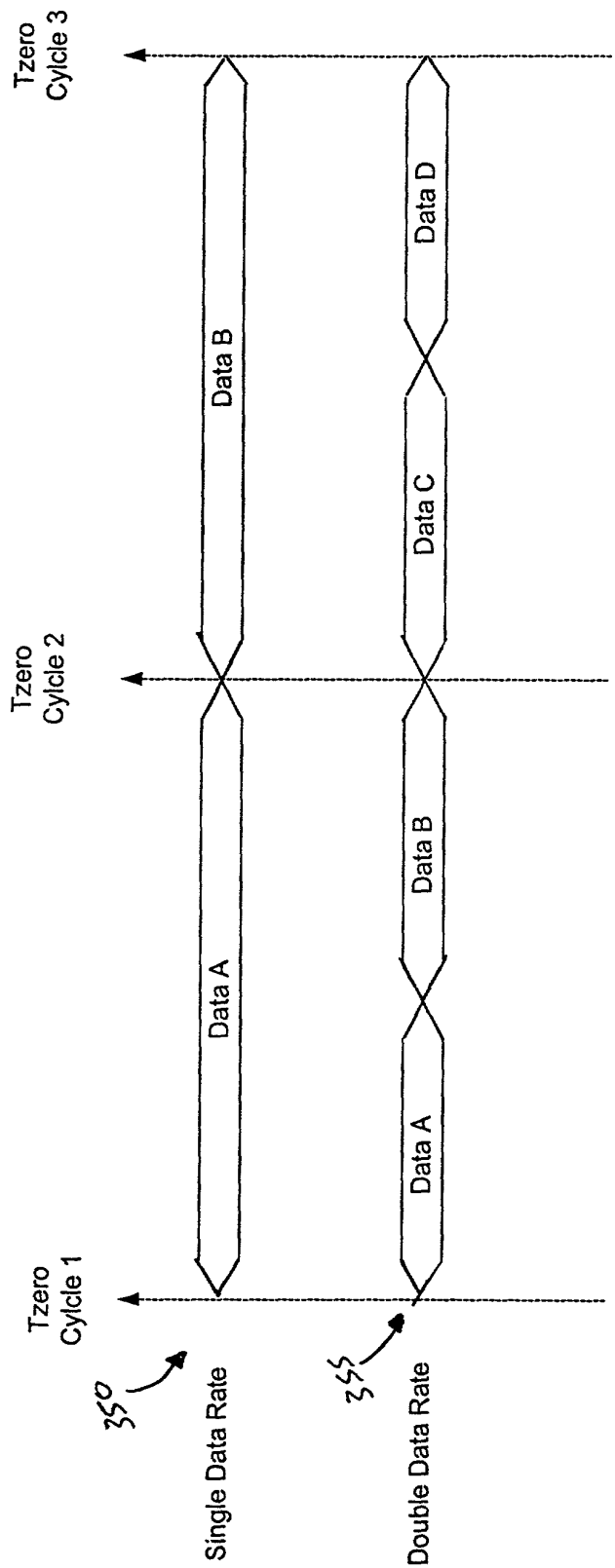


Fig. 7

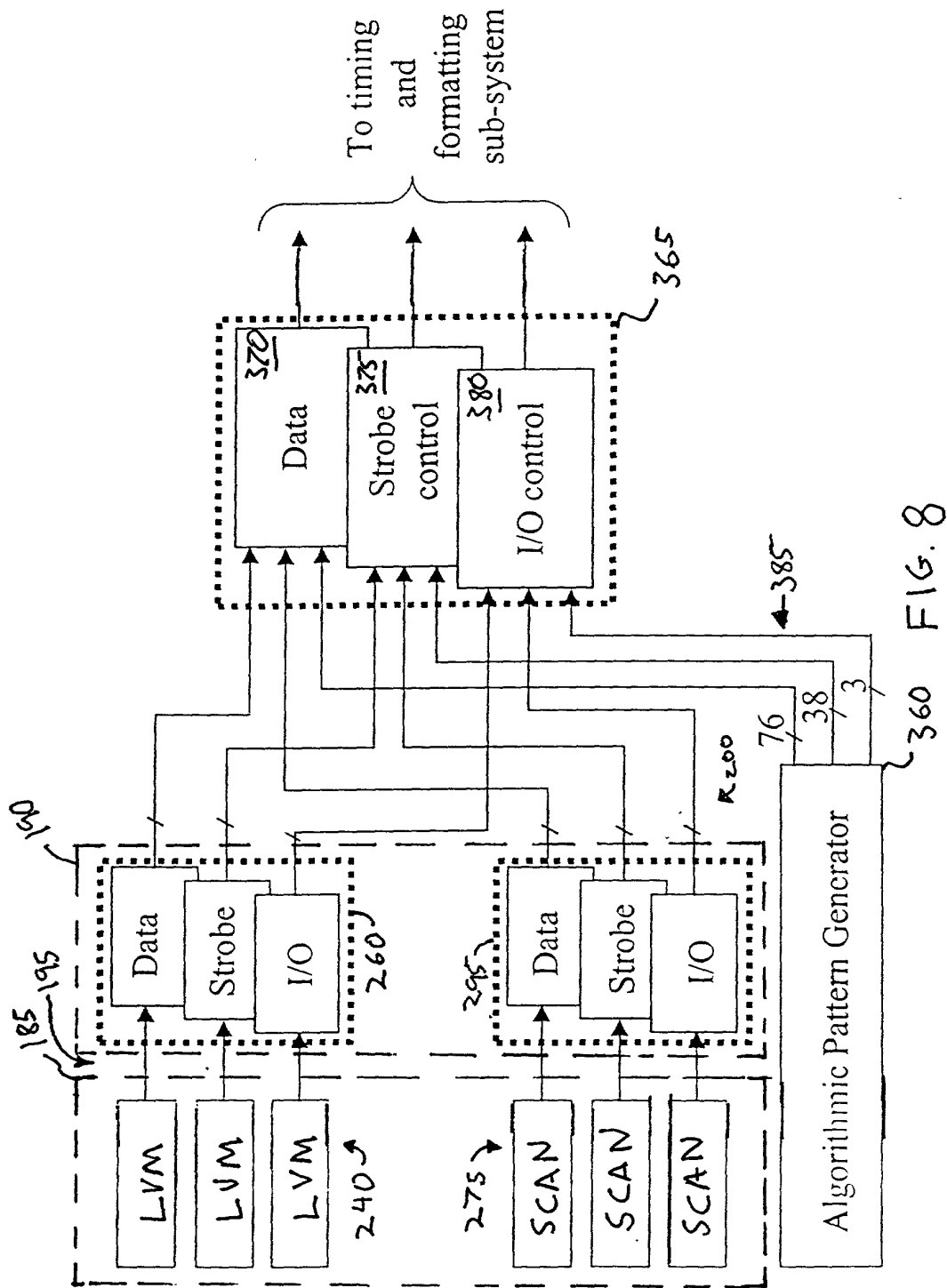


FIG. 8



STORE IN THE PATTERN MEMORY A TEST PATTERN INCLUDING A NUMBER OF BITS FOR TESTING THE DUT

~400

PROGRAM THE PATTERN SCRAMBLER TO COUPLE BITS FROM ONE OR MORE OF THE OUTPUTS OF THE PATTERN MEMORY TO ONE OR MORE OF THE PINS ON THE DUT, THEREBY PROVIDING A TEST PATTERN TO THE DUT

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COUPLE AN OUTPUT OR SIGNAL FROM THE DUT IN RESPONSE TO THE TEST VECTOR BACK THROUGH THE COMPARATOR AND ERROR LOGIC CIRCUIT

~410

OPTIONALLY LOG RESULTS IN AN ERROR CAPTURE MEMORY

~415

OPTIONALLY PROGRAM THE PATTERN SCRAMBLER TO CHANGE AT LEAST ONE OF THE WIDTH OR THE DEPTH OF THE TEST PATTERNS PROVIDED TO THE DUT ON A CYCLE-BY-CYCLE BASIS FOR EACH CLOCK CYCLE OF THE APPARATUS

~420

FIG. 9